# EZ-USB FX2™ PCB Design Recommendations

AN1196

Introduction

This application note presents recommendations for designing with the Cypress Semiconductor EZ-USB FX2™ component. Techniques for high-speed design should be applied to circuits using the EZ-USB FX2. Due to the packaging and high performance characteristics of the EZ-USB FX2, consideration of the PCB thermal design is required.

CY4611 EZ-USB FX2 USB to ATA Reference Design

A complete design using the Cypress CY7C68013 EZ-USB FX2 is available. The design implements the recommendations of this application note. It may be useful for the reader to download the CY4611 Reference Design Files from the Cypress Support page for Reference Designs.

Figure 1. FX2 (CY4611) USB to ATA Reference Design
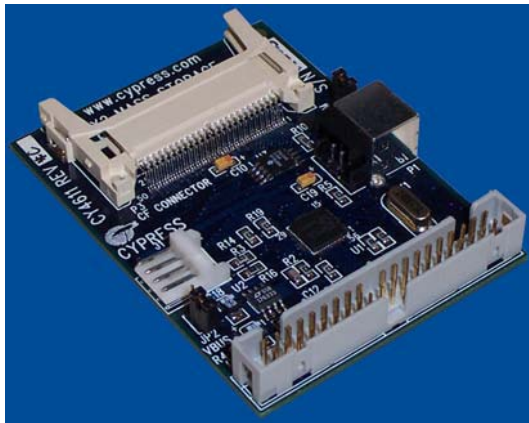
Cypress offers the CY4611 EZ-USB FX2 USB to ATA Reference Design as an evaluation platform for developers wishing to integrate a USB 2.0 Peripheral Controller into their application. The kit includes the EZ-USB FX2 USB to ATA evaluation board, USB cable, schematics, bill of material, PCB Gerber files, and other documentation.

EZ-USB FX2 Package Description

The CY7C68013-56LFC EZ-USB FX2 component is packaged as a 56-pad, 8-mm by 8-mm, 1-mm high, QFN (Quad Flatpack No leads) package. Please refer to the latest CY7C68013 EZ-USB FX2 USB Microcontroller High-speed USB Peripheral Controller data sheet for the detailed package drawing. The data sheet is Cypress specification 38-08012.

This package is comparable to the Amkor MicroLeadFrame™ package. It is a plastic encapsulated, near-chip scale package using solder lands instead of leads or balls. It uses a copper leadframe substrate that provides for short die to frame lead length giving good high-frequency performance. It has an exposed die paddle that enables good thermal transfer out of the package. For further details about this package and methods and processes associated with its assembly to a printed circuit board, please refer to the manufacturer's application note identified in the References section of this document.

Electrical Design Recommendations

USB 2.0 high-speed signaling is used to transfer data at 480 Mbps. This rate is 40 times higher than the highest speed of the USB 1.1 specification, full-speed signaling that operates at a 12-Mbps rate. High-speed signaling requires a greater level of attention to electrical design than previously required for USB designs. Careful attention to component selection, supply decoupling, signal line impedance, and noise are required when designing for high-speed USB. These physical issues are mostly effected by the PCB design and is presented in the PCB Design Recommendation section.

One key measurement of USB data signal quality is the eye pattern. The eye pattern is a representation of USB signaling that provides minimum and maximum voltage levels as well as signal jitter. Section 7.1 in the USB 2.0 Specification provides detailed explanation and requirements for a compliant eye pattern. Figure 2 is an eye diagram of high-speed signaling as measured on the EZ-USB FX2 component.

Figure 2. FX2 Eye Diagram of High-speed Signaling
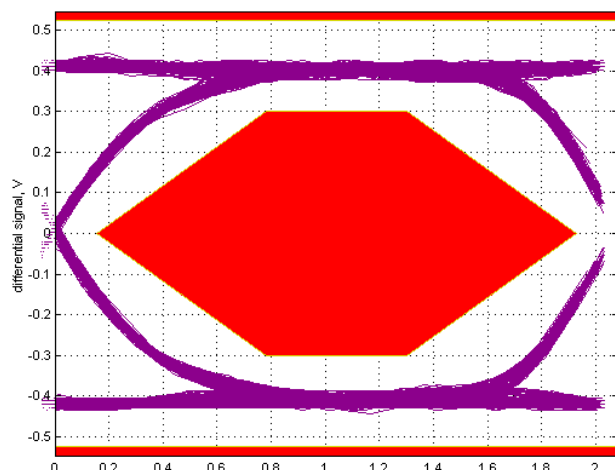
In the diagram, notice how no signal traces overlap the central, six-sided, shaded area. Also, no trace overlaps the extremes of permissible voltage as shown in the shaded lines at the very top and very bottom of the figure. Overlap of signal trace over the shaded areas would be a violation of the USB 2.0 specification. Overlap can be caused by excessive data jitter, mismatched impedance, and improper EMI filtering.

The Cypress Semiconductor application note titled "High-Speed USB PCB Layout Recommendations" treats the electrical design concerns applicable to high-speed USB 2.0 circuits. There are numerous textbooks that treat the subject of high-speed design in general. One such book is listed in the References section of this document.

EZ-USB FX2 Device Supply Decoupling

Decoupling capacitors should be ceramic type of a stable dielectric. For lower value capacitance, it is appropriate to use Class 1 dielectric capacitors, C0G (also referred to as NPO). Class 2 X7R should be used for the larger values. It is recommended that 0.01-µF and 0.001-µF capacitors be used to decouple supply pins nearest the pair of USB transceiver circuits. The 0.001-µF should be C0G dielectric. This will help decouple the power supply at the frequency range of high-speed USB switching. The other power supply pins should be decoupled with 0.1-µF X7R capacitors. It is important to have short trace runs for the power and ground connections from the EZ-USB FX2 component to solid power and ground planes.

The specific recommendation for the ceramic capacitor nearest each EZ-USB FX2 power pin is given in Table 1 below.

Table 1. Capacitor Recommendation

QFN Pin Number	Capacitor Value	QFN Pin Number	Capacitor Value
7	0.01 µF	43	0.1 µF
11	0.001 µF	55	0.1 µF
17	0.1 µF	3	0.1 µF
27	0.1 µF	3	2.2 µF
32	0.1 µF		

EMI and ESD Considerations

EMI and ESD need to be considered on a case by case basis relative to the product enclosure, deployed environment, and regulatory statutes. This application note does not give specific recommendations regarding EMI, but only gives general EMI and ESD.

The CY7C68013 requires an external 24-MHz crystal. The component includes circuitry to step up that frequency to support the 480-MHz bit rate of high-speed USB signaling. Solid ground planes and short connections help keep emissions low. Common mode chokes on the USB data pair reduce emissions at the expense of signal quality. Other forms of EMI filtering such as insertion of ferrite beads in-line with USB data lines and addition of capacitance to the data lines are strongly discouraged as these may cause a significant corruption of signal quality.

An example of ESD consideration is in the coupling between signal and safety/shield ground. The two grounds can be coupled together with the parallel connection of a 4.7-nF, 250VAC capacitor and a 1M-ohm resistor. Review the CY7C68013 data sheet regarding ESD susceptibility (the maximum static discharge voltage) for the component pins.

When USB type B connectors are used, they should be USB 2.0 compliant. These shielded connectors are designed with consideration for both EMI and ESD at the high-speed signalling rates. In this connector the safety/shield ground is kept separate from the signal ground.

PCB Design Recommendation

Printed circuit board (PCB) design for high-speed signaling requires careful attention to component placement, signal routing, layer stack-up, and selection of board material. These characteristics impact electrical signal quality of the USB data pair and the efficient dissipation of heat from the EZ-USB FX2 component.

Some areas of special note concerning design with high-speed devices are addressed in this section.

Maintain PCB Trace Impedance

Designing the PCB traces for particular characteristic impedance is very important to signal quality. The USB specification requires controlled impedance among all elements in the USB data path. The differential impedance of each USB data pair should be 90 ohms with a 10% tolerance to match the differential output impedance of high-speed capable drivers.

A common way to implement a differential pair is to use an edge-coupled, surface micro-strip line. The pair is placed on the board's surface layer, and is directly over a ground plane layer. This is the scenario used in the design of the CY4611. The following five parameters set the value for the differential impedance.

Table 2. Parameters for Differential Impedance

Term	Description
h	Height of signal traces above ground plane
ε_r	Material dielectric constant
t	Trace thickness
w	Trace width
s	Spacing between each trace of a differential pair, inside edge-to-edge

Parameters **h**, **t**, **w**, and **s** may be any unit but must be consistent. For example, the CY4611 design referenced in this application note shows these units in mil, (an English unit, 1/1000th of an inch). ε_r is a dimensionless constant.

For an edge-coupled, surface micro-strip, these five parameters (**h**, ε_r, **t**, **w**, and **s**) set the value for the differential impedance ("**Zdiff**"). **Zdiff** is defined in terms of the impedance of each line of the pair, ("**Z_0**"). The equations approximating impedance are:

$$Zdiff = 2 \cdot Z_0 \cdot \left(1 - 0.48 \cdot e^{-0.96 \cdot \frac{s}{h}} \right) ohms \qquad \text{Equation 1}$$

$$Z_0 = \left(\frac{87}{\sqrt{\varepsilon_r + 1.41}} \right) \cdot In \left(\frac{5.98 \cdot h}{0.8 \cdot w + t} \right) ohms \qquad \text{Equation 2}$$

The above equations yield a good estimate of **Z_0** and **Zdiff** when the following conditions are true:

$$\left(\frac{w}{h} \right) \le 2.0$$

$$0.20 \le \left(\frac{s}{h} \right) \le 3.0$$

The reference section lists a book resource and cites a URL for downloading a spreadsheet for calculating the impedances mentioned. The following is an example of calculating the trace impedance that is used in the CY4611 FX2 USB to ATA/CF Reference Design.

Table 3, which is extracted from the CY4611 FX2 USB to ATA/CF Reference Design drawings, shows the dimensions that impact the impedance for the USB data traces. These dimensions must not only satisfy the required characteristic impedance but must also be applicable in a practical physical design. For instance, different fabrication processes may have limited choices for material dielectric constant and material thickness between the signal layer and the ground layer. These two parameters dictate the trace dimensions for this design. The PCB manufacturer's material for the PCB was taken from their standard supply. The vendor provided the tolerance values shown in Table 3. The values are all finished dimensions.

Table 3. Tolerance Values

|	Tolerances	Min.	Nominal	Max.
Material Thickness(mils)	±1.0	9.7	10.7	11.7
Material Dielectric	±0.2	3.8	4.0	4.2
Trace Thickness, 1 oz. (mils)	±0.1	2.3	2.4	2.5
Width (mils)	±0.5	16.75	17.25	17.75
Spacing (mils)	±1.0	12.75	13.75	14.75

Using the dimensions from Table 3, the **Zdiff** for the USB data pairs of the CY4611 FX2 USB to ATA/CF Reference Design is 90 ohms +0%, –4%.

The designer should take advantage of any help available from the PCB manufacturer. The key dimensions and tolerances should be available from the manufacturer. Some manufacturers will perform the impedance calculations for the designer. Some will provide a service to measure the impedance after the PCB is fabricated.

PCB Layer Stack-Up

For best signal characteristics, a USB 2.0 high-speed design requires at least a four-layer PCB. It is recommended to place the primary components (CY7C68013 and its crystal) on the first (or top) layer, followed by the solid signal ground plane. The third layer should be the voltage plane followed by the fourth bottom layer. Figure 3 below illustrates these 4 layers which are used in the PCB for the CY4611 FX2 USB to ATA/CF Reference Design.

Figure 3. Recommended PCB Stack-up
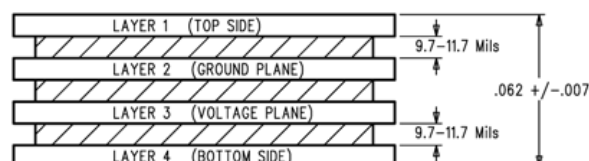
This figure shows the dielectric material thickness ("Prepreg") between layers 1 and 2 and the thickness between layers 3 and 4. The dimensions between these layers are a key element in the design to set the proper characteristic impedance for the USB data traces. This is the "h" term mentioned in the prior section on PCB impedance design. The core material of the PCB lies between layer 2 and 3. Although this material is not critical to impedance characteristics, it is used to determine the overall board thickness.

Split Planes and Signal Routing

The shield/safety ground is on one of the four layers of the PCB. However, when viewed across all layers of the PCB, the section with the shield/safety ground plane should not overlap any other planes or signals. If the shield/safety ground is on the edge of the board with the USB connectors, then there should not be any other metal in other PCB layers directly above or below that area.

An alternate method of isolating the shield from the signal ground is shown is Figure 4. The lower section of Figure 4 illustrates a portion of the ground layer. Given this scenario, shield/safety ground plane is on the same layer as the signal ground plane and is associated with the PCB's layer two.

Figure 4. Section of Split Ground Plane
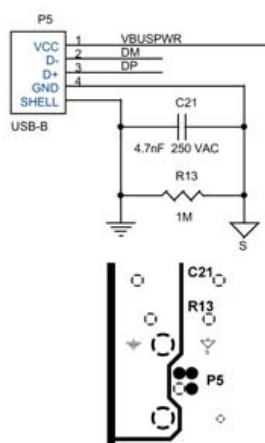
The upper portion of Figure 4 shows the schematic associated with the coupling across a split plane using C21 and R13 components. The width of the gap between the shield/safety ground and the signal ground should be no less than 25 mil in order to minimize electrical edge coupling.

It is not necessary to have a large shield/safety ground plane. A 100-mil-wide trace for interconnect is sufficient.

The following is a list of routing requirements which should be adhered to:

- USB connector pins 1, 2, 3, and 4 are in the area of the signal ground, not the shield/safety ground.

- The USB signals traces from the connector route over the signal ground plane, never over the shield/safety ground.

- No signal should route over the shield/safety ground plane.

- No other power or signal ground planes should overlap the shield/safety ground plane.

- All USB data signals should be routed exclusively on layer one, the top side.

- They should not route underneath any component except for their associated USB connector.

- Line length should be minimized.

- To minimize coupling between the USB data pair and other non-USB signals, the USB data pair should not be closer than 35 mil to another signal.

- If a ground fill is to be used on the top side of the board, then to avoid significant impact to signal impedance, the USB data pair should not be within 35 mil of the surface ground plane.

These guidelines also apply to the crystal used for the CY7C68013.

USB data lines must maintain proper differential pairing. This is not possible at either end of the trace. At either end of the trace, the physical limitation of routing to the pins of the USB connector and the CY7C68013 causes a divergence from this.This divergence should be minimized and the signal pairs should adhere to the proper trace design for the required 90-ohm differential impedance.

Thermal Design Considerations

The QFN (Quad Flatpack No leads) is a package with a small footprint and low profile. It has excellent thermal properties: a very low Θ_{ja} of approximately 25°C per watt. These thermal properties are ideal for the high-performance FX2.

The appropriate thermal design for use with the EZ-USB FX2 is to dissipate heat from the QFN package by conduction, not convection. Heat is conducted away from the package through its bond to the PCB. From there it is dissipated into the signal ground plane. Special attention to the heat transfer area below the package is required.

On the bottom of the package is a metal pad referred to as the exposed die attach paddle, (or simply exposed paddle). The exposed paddle is the means by which most of the EZ-USB FX2 thermal energy is dissipated away from the package. The exposed paddle is a square metal area approximately 6 mm on a side.

The design of the land area for the exposed paddle is critical to proper thermal transfer. A copper fill is to be designed into the PCB and under the QFN in order to assist thermal transfer. Figure 5 is the diagram of the PCB land area for the EZ-USB FX2.

Figure 5. Diagram of the PCB Land Area
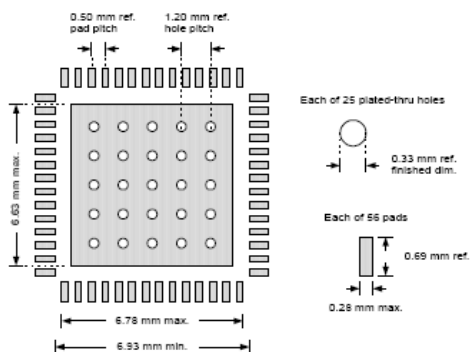
The heat is transferred to the solid signal ground plane of the board. The connection is made using a 5 x 5 array of 25 plated through-holes in the PCB; each should have a finished diameter ranging from 12 mil to 13 mil. Solder mask is placed over the top of each plated through-hole to resist solder flow into the hole. The mask also is used to create voids in the flowed solder for out-gassing during the solder reflow process.

Research done by Amkor, a package manufacturer, has determined that an array of more than 16 and less than 36 plated through-holes should be used for the PCB land for the exposed paddle. Figure 6 shows the trend in Θ_{ja} with respect to the number of vias. This specific graph show the trend on Amkor's 7 mm 48-lead package. The result shows that the thermal efficiency improves with increase in the number of plated though holes. A lower Θ_{ja} indicates a better thermal efficiency. The results obtained on the Amkor part can be extrapolated to the EZ-USB FX2.

Figure 6. Thermal Efficiency
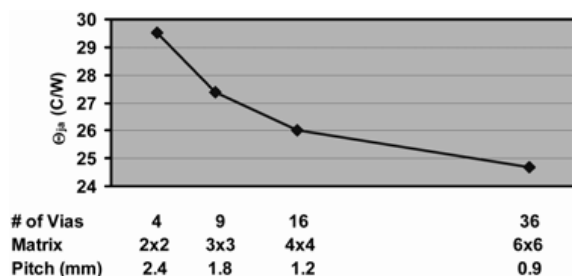
Figure 7 shows the solder mask region at the package. Each of the 25 plated through-holes is in the center of each circle of solder mask. Black area indicates absence of solder mask.

Figure 7. Solder Mask
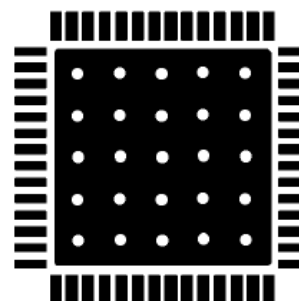
The signal ground plane provides the major area for thermal dissipation. The CY4611 uses the large internal layer of the PCB devoted to signal ground. This is a fairly large board intended for demonstration and evaluation of the CY7C68013 component.

For a fielded product, some developers may need a much smaller board size than the CY4611. To maximize area devoted to thermal dissipation, the designer should use the bottom layer of the PCB. This is in addition to the internal solid ground plane, (which must be kept to maintain proper signal impedance). The metal fill must be connected to the signal ground plane at each of the 25 plated through-holes under the QFN mounting. Additional 13-mil plated through-holes may be placed throughout the board to connect to the internal signal ground plane as desired. Most holes should be placed as close to the QFN package as practical to improve thermal transfer.

The enclosure for the circuit board assembly affects thermal performance. This application note does not give a specific example of enclosure design. However, following the guidelines for PCB design described in this application note will assure the most efficient method to conduct heat away from the QFN package without the use of heat sinks. A large, solid ground plane with no large gaps close to the QFN mounting area will efficiently conduct heat through the PCB.

For further details on this package and methods and processes associated with its assembly to a printed circuit board, please refer to the manufacturer's application note for the package. It is identified in the References section of this document.

EZ-USB FX2 Assembly Recommendations

The solder stencil over the exposed paddle is required to permit at least 50% solder application coverage. Figure 8 is a graph from Amkor research showing how solder void much less than 50% has little influence on thermal transfer. The package is a smaller one than the EZ-USB FX2 8-mm 56-lead package, but the values do scale.

Figure 8. Thermal Performance versus Solder Void
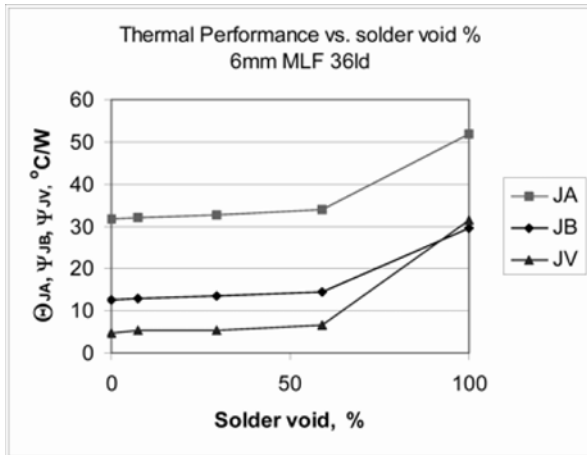
The manufacturing processes and practices of the assembly operation govern the stencil pattern used. Generally, arrays of either round or square patterns are used. A circular stencil was used for one assembly run of boards.

Figure 9. Stencil Area
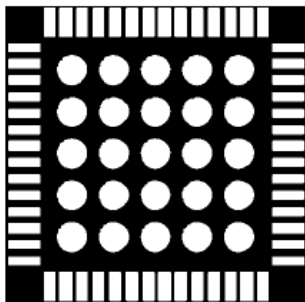
Figure 9 shows that the stencil area contains 25 holes. The holes are 1 mm in diameter on a 1.25-mm pitch. The pad land on the PCB is 6 mm square. This results in a solder coverage of approximately 54 percent. A stencil could have fewer holes but they would need to be larger and may not meet the minimum 50% coverage requirement. A large pattern of four squares could also be used. However, the larger the opening of each hole or square the more likely solder sputtering or out-gassing problems will occur. A solder stencil thickness of 0.125 mm is recommended for this package. Figure 10 below displays a cross-sectional area underneath the package. The cross section is of only one via and is the recommended dimensions for the via.

Figure 10. Cross-section Area of via
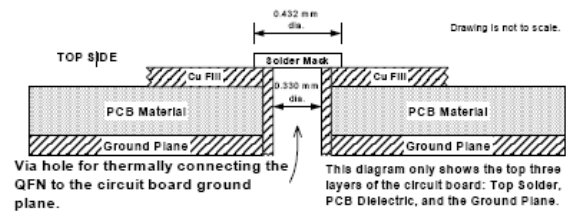
Since there is no space under the package after soldering, it is recommended to use a "No Clean," type 3 solder paste.

Nitrogen purge is recommended during solder reflow.

Summary

Following the recommendations of this application note should help the designer to produce a compliant and high-performance USB 2.0 device design. Compliance can be confirmed with testing at the often-scheduled USB-IF Compliance Workshops. To the extent possible, developers of USB products should test their designs for compliance prior to attending one of the Workshops.

References

Cypress, *CY4611 FX2 USB to ATA/CF Reference Design Kit*, Cypress Semiconductor, California, 2002.

Cypress, Cypress Semiconductor web site, www.cypress.com/, Cypress Semiconductor, California.

USB-IF, *Universal Serial Bus Specification, Revision 2.0*, USB Implementers Forum, Oregon, 2000.

USB-IF, *USB Developers web site*, www.usb.org/developers/, USB Implementers Forum, Oregon.

Amkor, *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame™ (MLF™) Packages*, Amkor Technology, Pennsylvania, 2002. URL at the time of this writing

www.amkor.com/prodcts/notes_papers/MLF_AppNote_0902.pdf

Amkor, *Amkor Technology web site*, http://www.amkor.com/, Amkor Technology, Pennsylvania.

PCB Standards, Impedance Calculator, pcbstandards.com, California, 2002. At the time of this writing the URL is www.pcbstandards.com/downloads/Metric%20Environment/Calculators/Impedance/Impedance%20Calculator.xls

PCB Standards, *PCB Standards web site*, www.pcbstandards.com/, California.

Howard W. Johnson, *High-Speed Digital Design: A Handbook of Black Magic*, Prentice Hall PTR, New Jersey, 1993, ISBN 0-13-395724-1.

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